	Type	L #	Hits	Search Text	DBs
1	BRS	L2	2012	(channel near region) near25 (gate near dielectric)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
2	BRS	L3	60106	"1" and (remov$3) near15 (sidewall$1 or side near wall$1 or spacer$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
3	BRS	L4	507	2 and (remov$3) near15 (sidewall$1 or side near wall$1 or spacer$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
4	BRS	L5	153	2 and ((substrate) near35 (remov$3) near15 (sidewall$1 or side near wall$1 or spacer$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
5	BRS	L6	0	(channel near region) near25 (gate near dielectric) near25 (gate near3 mandrel)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
6	BRS	L7	0	(channel near region) near25 (gate near dielectric) near25 (mandrel)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
7	BRS	L8	1	(channel near region) near25 (gate) near25 (mandrel)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
8	BRS	L9	114	(gate near3 mandrel)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
9	BRS	L10	19	(gate near3 mandrel) near25 (spacer$1 or sidewall$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
10	BRS	L11	0	(gate near3 mandrel) near25 (side near wall$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
11	BRS	L12	1231	(mandrel) near25 (side near wall$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
12	BRS	L13	2585	(mandrel) near25 (spacer$1 or sidewall$1)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	Type	L #	Hits	Search Text	DBs
13	BRS	L14	74	13 and ((sourece or drain) near (region))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
14	BRS	L15	92	13 and ((source or drain) near (region))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
15	BRS	L16	41	13 and ((source) near (region))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB
16	BRS	L17	16	(fill$3) near35 ((gate near dielectric) near5 (side or plat$1))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB

	U	1	Document ID	Title
1			US 20050009305 A1	METHOD OF FORMING FREESTANDING SEMICONDUCTOR LAYER
2			US 20020109179 A1	SELF-ALIGNED NON-VOLATILE RANDOM ACCESS MEMORY CELL AND PROCESS TO MAKE THE SAME
3			US 20020028554 A1	Formulation of multiple gate oxides thicknesses without exposing gate oxide or silicon surface to photoresist
4			US 20020011608 A1	Self aligned method of forming a semiconductor memory array of floating gate memory cells, and a memory array made thereby
5			US 6593177 B2	Self aligned method of forming a semiconductor memory array of floating gate memory cells, and a memory array made thereby
6			US 6552378 B1	Ultra compact DRAM cell and method of making
7			US 6525371 B2	Self-aligned non-volatile random access memory cell and process to make the same
8			US 6344381 B1	Method for forming pillar CMOS

	U	1	Document ID	Title
9			US 6339001 B1	Formulation of multiple gate oxides thicknesses without exposing gate oxide or silicon surface to photoresist
10			US 6329685 B1	Self aligned method of forming a semiconductor memory array of floating gate memory cells and a memory array made thereby
11			US 6255699 B1	Pillar CMOS structure

	U	1	Document ID	Title
12			US 6252267 B1	Five square folded-bitline DRAM cell
13			US 6100123 A	Pillar CMOS structure
14			US 6090660 A	Method of fabricating a gate connector
15			US 6037620 A	DRAM cell with transfer device extending along perimeter of trench storage capacitor
16			US 5893735 A	Three-dimensional device layout with sub-groundrule features

	U	1	Document ID	Title
17			US 4833094 A	Method of making a dynamic ram cell having shared trench storage capacitor with sidewall-defined bridge contacts and gate electrodes
18			US 4785337 A	Dynamic ram cell having shared trench storage capacitor with sidewall-defined bridge contacts and gate electrodes
19			US 5893735 A	Three dimensional cell forming process for dynamic random access memory (DRAM)